In the Claims:

Please amend claims 1, 8, 13 and 14. Please cancel claims 15-20. Please add new claims 21-27. The claims are as follows:

- 1. (Currently Amended) A method, comprising:
 - (a) providing a substrate;
 - (b) forming a first single-crystal layer on a top surface of said substrate;
 - (c) forming a second single-crystal layer on a top surface of said first single-crystal layer;
 - (d) forming one or more devices in said second single-crystal layer;
- (e) forming a trench in said second-single crystal layer, said trench surrounding said one or more devices, to form a single-crystal island containing said one or more devices in a region of said second single-crystal layer, said first single-crystal layer exposed in a bottom of said trench; and
- (f) removing said first single-crystal layer in order to separate said single-crystal island from said substrate.
- 2. (Original) The method of claim 1, wherein step (f) includes selectively removing said first single-crystal layer with respect to said second-single crystal layer.
- 3. (Original) The method of claim 1, wherein said substrate comprises silicon.
- 4. (Original) The method of claim 1, wherein said first single-crystal layer comprises Si_xGe_y , Si_xC_y or Si_xAs_y .

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- 5. (Original) The method of claim 1, wherein said second single-crystal layer comprises silicon.
- 6. (Original) The method of claim 1, further including:
 - (g) after step (f) repeating steps (a) through (f) one or more times.
- 7. (Original) The method of claim 1, further including:
- (g) after step (f) mechanical-chemical-polishing said substrate to expose a new top surface of said substrate; and
 - (h) after step (g) repeating steps (a) through (g) one or more times.
- 8. (Currently Amended) The method of claim 1, further including:

between steps (e) and (f), forming a spacer on a sidewall peripheral sidewalls of said single crystal island.

- 9. (Original) The method of claim 1, wherein said one or more devices are independently selected from the group consisting of NFETS, PFETs, bipolar transistors, resistors and capacitors.
- 10. (Original) The method of claim 1, wherein step (d) further includes interconnecting said one or more devices to form an integrated circuit in said second-single crystal layer.

- 11. (Original) The method of claim 10, wherein said integrated circuit is a radio frequency identification circuit.
- 12. (Original) The method of claim 1, wherein said trench comprises one or more intersecting trenches.
- 13. (Currently Amended) A method, comprising:
 - (a) providing a single-crystal substrate;
 - (b) forming a buried single-crystal layer in said substrate;
- (c) forming one or more devices in said a layer of said single-crystal substrate above said buried single-crystal layer;
- (d) forming a trench <u>surrounding said one or more devices in a region of</u> said layer of said single-crystal substrate above said buried single-crystal layer to form a single-crystal island containing said one or more devices, said buried single-crystal layer exposed in a bottom of said trench; and
- [[(f)]] (e) removing said buried single-crystal layer in order to separate said single-crystal island from said substrate.
- 14. (Currently Amended) The method of claim 13, wherein step (b) includes performing an ion implantation of Ge or As <u>or C</u> followed by performing a heat treatment.

15-20 (Canceled)

- 21. (New) The method of claim 13, wherein said substrate comprises silicon.
- 22. (New) The method of claim 13, wherein said first single-crystal layer comprises Si_xGe_y , Si_xC_y or Si_xAs_y and said second single-crystal layer comprises silicon
- 23. (New) The method of claim 13, wherein said one or more devices are independently selected from the group consisting of NFETS, PFETs, bipolar transistors, resistors and capacitors.
- 24. (New) The method of claim 13, wherein step (d) further includes interconnecting said one or more devices to form an integrated circuit in said second-single crystal layer.
- 25. (New) The method of claim 24, wherein said integrated circuit is a radio frequency identification circuit.
- 26. (New) The method of claim 13, wherein said trench comprises one or more intersecting trenches.
- 27. (New) A method, comprising:
 - (a) providing a substrate;
 - (b) forming a first single-crystal layer on a top surface of said substrate;
 - (c) forming a second single-crystal layer on a top surface of said first single-crystal layer;
 - (d) forming one or more devices in said second single-crystal layer;

- (e) forming a trench in said second-single crystal layer to form a single-crystal island containing said one or more devices, said first single-crystal layer exposed in a bottom of said trench; and
- (f) removing said first single-crystal layer in order to separate said single-crystal island from said substrate.